Technical Field

This invention relates to the field of semiconductor materials, and in particular, to the growth of semiconductor crystals.

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Background of the invention

An obstacle in realizing next-generation microelectronic and optoelectronic devices and optimal

10   integration of these devices is found in lattice mismatches between different crystals of group III-V semiconductor materials. Generally, the lattice mismatch between a substrate and an epitaxial over-layer induces strains within the over-layer. This may lead to strain relaxation which can result in formation of material defects such as dislocations within the crystalline structure of the over-layer. Fig.1 illustrates a mismatched over-layer 1 epitaxially grown over a substrate 2, the

15   boundary between the over-layer 1 and the substrate 2 being indicated with reference numeral 4. As shown in Fig. 1, the lattice constant associated with the over-layer 1 is different from the lattice constant associated with the substrate 2, hence the term "mismatched over-layer". Strain relaxation due to lattice mismatch is accommodated by the formation of mismatch dislocations 3 within the crystal. Defects within a crystal generally degrade the performance of devices made

20   from the crystal, because such defects can scatter movement of carriers (electrons and holes) and can act as carrier traps and/or recombination centers. It is thus useful to provide means for

growing a crystal over-layer which has different lattice constant from the substrate on which the

over-layer is grown, in such a fashion that strain relaxation does not occur and mismatch

dislocations do not form. Fig. 2 is an example of this, in which the structure of over-layer 1 is

preserved and no mismatch dislocations are formed.

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In the prior art, two main approaches are used to address the lattice mismatch problem and the

strain relaxation it causes :

1) In a first approach, defects are confined in thick relaxed buffers so that the top active

layer of a device can be of a different lattice constant from that of the substrate and is as defect

10   free as possible.

2) In a second approach, thin compliant solid layers are bonded to foreign substrates and

re-growth is performed.

However, these approaches still present performance degradation problems. A buffer layer of

15   defects degrades the quality of the active layer on top of the buffer layer used for a device. In

addition, thick buffer layers are not very suitable for device fabrication because high mesa or deep

isolation implants are then necessary for device isolation, and can result in high leakage currents

and low wafer yields. Further, procedures for implementing the second approach are rather

complicated due to problems associated with wafer bonding, fabrication of thin layers (tens of Å

20   in thickness) and re-growth on surfaces contaminated in the wafer-bonding and fabrication

processes.

Hence, there is a need for a method of growing a crystal over a substrate such that mismatch dislocations are prevented from appearing within the crystal, even though the crystal and the substrate have different lattice constants.

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Brief description of the invention

In accordance with this invention, compliant layers of group-V species are formed in situ, which distinguishes this invention from the prior art. Indeed, in this invention, formation of compliant layers does not require wafer-bonding and fabrication procedures performed outside of the growth chamber. Furthermore, crystals grown on top of compliant layers will not be strained and therefore, will not suffer strain relaxation which results in dislocation defects.

15   The present invention relates to processes and methods which facilitate the epitaxial growth of group III-V crystals of different lattice constants on top of each other. One object of this invention is to suppress strain relaxation associated with lattice-mismatched epitaxy. This is realized with a growth process that initially forms a substrate surface free of oxides. The growth process then deposits, at appropriately low growth temperatures, a layer of condensed group-V

20   species and a mono-layer of constituent group-III atoms in order for the crystal over-layer to retain the condensed layer. Subsequently, the mono-layer is annealed at a higher temperature.

Finally, the bulk of the crystal over-layer is grown with the condensed group-V layer accommodating the strain build-up which occurs during the bulk growth.

In one example of the lattice-mismatch growth process, the substrate may be gallium arsenide, the
5   condensed group-V species may be arsenic and the crystal over-layer to be grown may be indium arsenide (The lattice constant of indium arsenide differs from that of gallium arsenide by 7.2%).

In one aspect, the present invention relates to a semiconductor device comprising a substrate of a group-III/group-V material, a layer of a group-V material disposed over the substrate, a mono-
10   layer of group-III atoms disposed over the layer of group-V material, and a layer of a group-III/group-V crystal epitaxially grown over the mono-layer.

Brief description of the drawings

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Fig. 1 is a schematic representation of a mismatched layer where some of the strain has relaxed by the formation of mismatched dislocations within the grown upper layer;

Fig. 2 is a schematic representation of how lattice mismatch is accommodated by a condensed
20   layer of group-V species in accordance with this invention;

Fig. 3 is a schematic representation of the growth chamber illustrating desorption of surface

oxides from the surface of the substrate;

Fig. 4 is a schematic representation of the growth chamber illustrating the deposit of a first layer

5   of group-V species over the substrate;

Fig. 5 is a schematic representation of the growth chamber illustrating the deposit of a second

layer of group-III species over the first layer of group-V species;

10   Fig. 6 is a schematic representation of the growth chamber illustrating the epitaxial growth of a

crystal over the second layer;

Fig. 7 is a schematic representation of a semiconductor device in accordance with this invention;

and

15   Fig. 8 is a schematic representation illustrating an exemplary embodiment of a semiconductor

device in accordance with this invention.

Detailed description of the invention

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In accordance with this invention, the process or method of growing of a group III-V crystal on

top of another group III-V crystal (substrate), without introducing lattice-mismatch defects,

include the following steps :

Step 1 : Thermal desorption cleansing of the substrate

5   In a preferred embodiment, the material forming the substrate upon which the epitaxial over-layer

is to be grown may include GaAs, GaP, InAs or InP. As would be apparent to the skilled person,

other group III-V compounds or crystals may be used as well.

In this step, and as illustrated by Fig. 3, the substrate 7 is first heated inside a growth chamber 6,

10   to a temperature T_s, where T_s ranges from about 495°C to about 600°C. Vapor 8 comprising

group-V species (e.g., As_2, As_4, P_2, P_4 or other group-V members) is introduced in the growth

chamber 6 when the substrate 7 is heated. The pressure P of the vapor 8 introduced may range

from about 0.004 pa to about 0.012 pa, which pressure P is larger than the vapor pressure P_s of

the substrate 7 at temperature T_s. The temperature of the vapor 8 which is introduced in the

15   growth chamber 6, may range from about 300°C to about 1000°C. The substrate 7 is then

annealed under this over-pressure of group-V species vapor, at temperature T_s, and desorption

of surface oxides 9 from the substrate 7 takes place, with the surface oxides being removed from

the chamber by pump 20.

20   ### Step 2 : In situ introduction of condensed group-V species

As sown in Fig. 4, an ultra-thin layer 11 of condensed group-V species (layer 4 of Fig. 1) which, in a preferred embodiment may comprise As_2, As_4, P_2 or P_4, is then introduced in situ at a temperature T_c, which temperature is lower than the optimal growth temperature for epitaxy of the crystal which is to be grown. Temperature T_c may vary from about 30°C to about 250°C. In

5   this step, and as illustrated by Fig. 4, a vapor 13 comprising a group-V species is introduced onto the surface of the substrate 7 by opening shutter 19. When the temperature T_s of the substrate 7 is appropriately low (between about 30°C and about 250°C), and the pressure P_c of the group-V vapor 13 is adequate (about 0.004 pa to about 0.012 pa), condensation of the group-V species on the substrate 7 takes place. The thickness of the layer 11 of group-V species which condenses on

10   the surface of the substrate 7, can be controlled by varying the temperature T_s of the substrate 7. Indeed, the amount of desorption from the condensed layer of group-V species is dependent on the temperature. In other words, different thicknesses of the layer 11 can be achieved by varying the temperature T_s. The temperature T_s of the substrate 7 is preferably set such that the thickness of the layer of the group-V species falls into a range of several Å to a few tens of Å.

15   The desired thickness of the layer 11 is achieved as soon as the temperature T_s is reached, generally in a matter of seconds.

Step 3: Deposit of a mono-layer of group-III atoms on the group-V layer

A layer of group-III atoms 12 is then deposited over the group-V layer 11 previously deposited

20   on the substrate 7, as illustrated by Fig. 5. This layer 12 may be have a thickness ranging from

one atom to a few atoms. In the preferred embodiment, the layer 12 is a mono-layer of group-III

atoms. The layer of group-III atoms 12 may comprise In, Ga, Al or any combination of Ga, Al

and In. The deposit may be made by opening, for an appropriate duration of time (between about

1 second and about 3 seconds) the shutter 14 of the furnace 15 containing a vapor of group-III

5   atoms 17. This duration of time may vary according to the geometry of the shutter 14 and

furnace 15, and the evaporation rate of the group-III atoms introduced. The vapor of group-III

atoms is introduced at a temperature ranging from about 780° C to about 1250° C and at a

pressure of about 5×10^{-5} pa. In atoms are preferably introduced at a temperature of about 780°

C, Ga atoms are preferably introduced at a temperature of about 900° C, and Al atoms are

1 0   preferably introduced at a temperature of about 1200° C.

After introduction of the vapor of group-III atoms 17 in the growth chamber 6, the vapor of

group-III atoms 17 condenses on the surface of the substrate 7 above the layer of group-V atoms

11, forming a mono-layer of group-III atoms 12. At this stage the substrate 7 is kept at a

1 5   temperature T_d ranging from about 30°C to about 250°C and the pressure of the group-V vapor

13 which was introduced in step 2 is maintained around 0.008 pa. The mono-layer of group-III

atoms 12, is then annealed by raising the temperature of the substrate T_d to a temperature from

about 400°C to about 580°C, under a pressure of group-V vapor 13 of about 0.008 pa . Such

mono-layer of group-III atoms 12 has the property of changing the desorption tendency of the

2 0   group-V species layer 11 lying underneath, and allows retention of the group-V species layer 11

during the annealing phase, which precedes the actual epitaxial growth of the crystal at an optimal

growth temperature. The group-III atoms in the mono-layer 12 will seek lattice sites of a lower free energy during annealing, and will therefore form a propitious starting atomic plane for subsequent epitaxial growth. Because the bonding, between group-V molecules in the thin condensed layer 11 initially deposited, is much weaker than that between atoms of the solid

5   crystal to be grown, the group-V molecules will relocate during the subsequent epitaxy to accommodate the lattice mismatch between the solid substrate crystal 7 and the desired solid crystal over-layer.

Step 4: Epitaxial growth of crystal

10   Growth of bulk group III-V species layer 18 may then be initiated by opening again the shutter 14 of the group-III furnace 15 as illustrated by Fig. 6. Such group III-V species layer 18 may include InAs, $In_xGa_{1-x}As$, $In_xAl_{1-x}As$ or GaP, but other group III-V species may be contemplated as well. In a preferred embodiment, group-V species and group-III species are introduced in the growth chamber with the ratio of the group-V flux to the group-III flux being

15   maintained in the range of about 1.5 to about 3.

For the purpose of illustration, the method of growing a group III-V crystal on top of another group III-V crystal, without introducing lattice-mismatch defects, is described in the particular example where the substrate is GaAs, the thin-layer of group-V species is As_2, the mono-layer of

20   group-III atoms is indium, and the crystal epitaxially grown is InAs. This method comprises the following steps:

Step 1 : Thermal desorption cleaning of the substrate

In one embodiment of this invention, a GaAs substrate 7 is heated to about 600°C and annealed

for about 10 minutes under an As_2 vapor 8 at a pressure of about 0.008 pa, which pressure is

5   larger than the vapor pressure of GaAs at 600°C.

Step 2 : In situ introduction of condensed group-V species

In this step, the temperature of the substrate 7 is first allowed to drop or is cooled to about 110°

C while the substrate 7 is subjected to an As_2 vapor pressure 13 of about 0.008 pa, so that a

10   condensed layer 11 of As_2 is formed on the surface of the substrate 7. The As_2 condensed layer

11 is then thinned down to the desired thickness, which thickness is preferably around several

tens of Å or less, by then raising the temperature of the substrate 7 to about 250° C.

Step 3: Deposit of a mono-layer of group-III atoms on the group-V layer

15   In this exemplary embodiment, the desired number of group-III atoms per surface area forming

the mono-layer is approximately 6.5e14 cm^{-2}. The shutter 14 of the furnace 15 is opened to

introduce indium vapor 17 at 790°C so that a mono-layer of indium 12 is deposited over the

condensed As_2 layer 11 .When the group-III flux incident on the growth surface is about

6.5e14/2.2 $cm^{-2}s^{-1}$, the shutter is preferably opened for 2.2 seconds in order to obtain the desired

20   mono-layer of 6.5e14 cm^{-2} group-III atoms. The substrate temperature is kept at about 250° C

while still being subjected to a pressure of As_2 vapor 13 of about 0.008 pa. The temperature of

the substrate 7 is then raised to about 400°C while the As_2 pressure 13 inside the growth

chamber is maintained around 0.008 pa. The mono-layer of indium 12 is annealed when the

substrate temperature ramps from about 250°C to about 400°C. After this step, the conditions

5   are propitious for epitaxial growth of InAs, without introducing dislocation defects due to lattice

mismatch between the GaAs substrate and the InAs crystal.

Step 4: Epitaxial growth of crystal

Growth of bulk InAs layer 18 may then be initiated by reopening the shutter 14 of the indium

10   furnace 15. The temperature is maintained at the optimal epitaxial growth temperature for InAs,

between about 400°C and about 450°C, while the ratio of the group-V flux to the group-III flux

introduced, is preferably maintained around 2.5.

In the methods described above, the substrate 7 may be heated in any way known in the art,

15   including through contact heat diffusion or radiation heat transfer. In one embodiment, a tantalum

filament is heated up by inducing an electrical current through the filament. The filament is

preferably disposed adjacent the back of the substrate, such that the heated filament radiates

energy to the substrate. Heat shields may be disposed under both the substrate and the filament

in such a way that most of the heat radiated by the filament is efficiently transmitted to the

20   substrate.

A pump 20 may be used throughout the steps of the methods of the present invention in order to rid the growth chamber of unwanted residual vapors, including surface oxides.

In another aspect, the present invention relates to a semiconductor device as shown in Fig. 7. The

5   semiconductor 20 comprises a substrate 7 of a group-III/group-V material, a layer 11 of group-V material disposed over the substrate 7, a mono-layer 12 of group-III atoms disposed over the layer 11, and a layer 18 of epitaxially grown group-III/group-V crystal disposed over the mono-layer 12. In an exemplary embodiment of the semiconductor device 20 shown in Fig. 8, the substrate 7 is GaAs, the layer 11 is As_2, the mono-layer 12 is In, and the crystal 18 is InAs.

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Even though the present invention is described in connection with specific group-III and group-V elements, any combination of these elements may be used.

Having described the invention in connection with certain embodiments thereof, modifications

15   will certainly suggest themselves to those skilled in the art. As such, the invention is not to be limited to the disclosed embodiments except as required by the appended claims.